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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/501,045	02/09/2000	Glenn T. Colon-Bonet	10971158-1	3338
22879	7590	01/25/2005	EXAMINER	
HEWLETT PACKARD COMPANY P O BOX 272400, 3404 E. HARMONY ROAD INTELLECTUAL PROPERTY ADMINISTRATION FORT COLLINS, CO 80527-2400				DO, CHAT C
		ART UNIT		PAPER NUMBER
		2124		

DATE MAILED: 01/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/501,045	COLON-BONET, GLENN T.	
	Examiner	Art Unit	
	Chat C. Do	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 13 September 2004 and 28 December 2004.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1,2,7,8,10 and 23-32 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1,2,7,8,10 and 23-32 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date _____

4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____

5) Notice of Informal Patent Application (PTO-152)
 6) Other: _____

DETAILED ACTION

1. This communication is responsive to Amendment filed 09/13/2004.
2. Claims 1-2, 7-8, 10, and 23-32 are pending in this application. Claims 1 and 7 are independent claims. In Amendment, claims 1 and 7 are amended; claims 3-6, 9, and 11-22 are cancelled; and claims 23-32 are added. This Office action is made final.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 7-8, 23-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Knowles (U.S. 6,446,107).

Re claim 1; Knowles discloses in Figure 3 an apparatus (abstract) for performing the addition of propagate, kill, and generate recoded numbers (e.g. each pair of bits in Figure 3 are encoded as PKG for OR, AND, and XOR logic gate respectively), apparatus comprising: a circuitry configured to receive at least a first operand (e.g. PKG of a0 and b0), a second operand (e.g. PKG of a1 and b1), and a carry-in bit (e.g. Co input), the first and second operands comprising respective first and second propagate, kill, and generate recoded number representations of respective first and second binary operands (e.g. 6₀ as

k, 2_0 as p, XOR with a0 and b0 input is g; similarly for a1 and b1); a first carry-save adder (e.g. a mid portion including 8_1 AND gate and attached XOR gate which interfaces with all p, k, and g of a0-a1 and b0-b1) configured to add first operand (representation of a0 and b0) and second operand (representation of a1 and b1) to generate a third propagate, kill, and generate recoded number representation (e.g. k, p, g results of a0 and b0; g of a1 and b1) and a carry-out bit (e.g. output of second level OR next to 8_1 AND gate which carry to the next bit); and a modified carry-save adder (e.g. 8_0 , 10_0 , 24_0 , and 24_1) configured to receive the third propagate, kill, and generate recoded number representation from the first carry-save adder (all pkg from a0 and b0 and g of a1 and b1), and the carry-in bit from the circuitry (e.g. C_0), add the separate propagate, kill, and generate bits of the third propagate, kill, and generate recoded number representation with the carry-in bit to generate a sum value (e.g. S_0 , S_0') and a carry value (e.g. output of 10_0 to the next bit or S_1, S_1') wherein the circuitry provides the carry-out bit from the first carry-save adder at a first output and the carry value from the modified carry-save adder at a second output (Figure 3).

Re claim 7, it is a method claim of claim 1. Thus, claim 7 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 8, Knowles further discloses in Figure 3 logically combining comprises adding the third propagate, kill, and generate representation and the carry-in value (e.g. 8_0 , 10_0 , 24_0 , and 24_1).

Re claim 23, Knowles further discloses in Figure 3 the sum value is a function of the third propagate representation and the carry-in value (e.g. 24_0).

Re claim 24, Knowles further discloses in Figure 3 the sum value is the XOR combination of the third propagate representation and the carry-in value (e.g. 24₀).

Re claim 25, Knowles further discloses in Figure 3 the carry value is a function of the third propagate representation, the carry-in value, and the third generate representation (e.g. 24₁).

Re claim 26, Knowles further discloses in Figure 3 the carry value is the OR combination of the third generate representation with the combination of the third propagate representation and the carry-in value (e.g. 10₀).

Re claim 27, Knowles further discloses in Figure 3 the carry-out value is a function of the first and second generate representations (e.g. output of OR gate adjacent to 8₁).

Re claim 28, Knowles further discloses in Figure 3 the carry-out value is the OR combination of the first and second generate representations (e.g. output of OR gate adjacent to 8₁).

Re claim 29, Knowles further discloses in Figure 3 the circuitry provides the sum value at a third output (e.g. 24₀).

Re claim 30, Knowles further discloses in Figure 3 logically combining comprises a XOR combination of the third propagate representation and the carry-in value (e.g. 24₀).

Re claim 31, Knowles further discloses in Figure 3 of logically combining comprises an OR combination of the third generate representation with the AND combination of the third propagate representation and the carry-in value (e.g. 8₀ and 10₀).

Re claim 32, Knowles further discloses in Figure 3 step of generating comprises an OR combination of the first and second generate representations (e.g. output of OR gate adjacent to 8₁).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 2 and 10 are rejected under 35 U.S.C. 103(a) as being obvious over Knowles (U.S. 6,446,107) in view of Miller (U.S. 5,706,323).

Re claim 2, Knowles does not disclose sum value and carry value are dual rail encoded values. However, Miller discloses a method of encoding variables into dual rail values in Figure 3. Therefore, it would have been obvious to a person having ordinary skill in the art to encode the sum value and carry value as dual rail values as seen in Miller's invention into Knowles' invention because it would simplify the circuitry and reduce the noise.

Re claim 10, it is a method claim of claim 2. Thus, claim 10 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Response to Arguments

7. Applicant's arguments with respect to claims 1-2, 7-8, 10, and 23-32 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2124

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2124

January 12, 2005

Varan. Ma.

KAKALI CHAKI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100